

REMARKS

The Amendments

Claims 1-33 and 136 are pending. Claims 34-135 are withdrawn. New Claim 136 is added. Claim 1 is amended to recite "directly on the top layer". Support for this amendment is found in the specification, for example, in Figure 1a. Support for new Claim 136 is found in the specification, for example, in Figure 1b. No new matter is added by the amendment.

The Response

Rejections Under 35 USC § 102

Claims 1, 10-14, 17, 22-24 and 30 are rejected under 35 U.S.C. 102(b) for allegedly being anticipated by Linliu et al. (U.S. Patent No. 6,110,837). Applicants respectfully traverse this rejection.

Claim 1 is directed to a method of fabricating a nanostructure array comprising: providing a substrate having a top layer, depositing a sacrificial layer having a first etching characteristic directly on the top layer, patterning the sacrificial layer, forming a thin conformal layer having a second etching characteristic over the patterned sacrificial structure, wherein the first and second etching characteristics are different, anisotropically etching the conformal layer to create a pattern, removing the sacrificial layer, **transferring the resulting conformal layer structure to the substrate by etching**, and removing any remaining conformal layer structure, thereby creating at least one nanostructure in the top layer. Claims 10-14, 17, 22-24 and 30 depend from Claim 1.

Linliu et al. disclose a method of forming structures consisting of a silicon oxide layer 130 over a polysilicon layer 120 that is on the surface of a gate oxide layer 110 which in turn is over a semiconductor substrate 100 (see Figure 8). Linliu et al. disclose removing the polymer layer 210 and polymer layer 220 to form the structures consisting of the silicon oxide layer 130 (col. 5, lines 27-35). However, it can be clearly seen by comparing Figures 6 and 7 that removing polymer layers 210 and 220 does not transfer the resulting structure of polymers layer 210 and 220 to the substrate.

Applicants contend that Linliu et al. do not teach the step of transferring the resulting conformal layer structure to the substrate by etching. The Examiner asserts that 210 of Fig. 2 of Linliu et al. is "a thin conformal layer" and 120 and 130 of Fig. 1 of Linliu et al. are "a top layer" (page 3). One can clearly see from Fig. 6 (shown below) that the structure of the asserted "thin conformal layer" (210) does not correspond to that of the asserted "top layer" (130). Linliu et al. state: "The polymer islands is consisted [sic] of the polymer layer 210 and the polymer 220 stand on the silicon oxide layer 130 and the polysilicon layer 120" (col. 5, lines 10-13; emphasis added). The structure of the asserted "thin conformal layer" (210) is at best a subset of that of the asserted "top layer" (130).

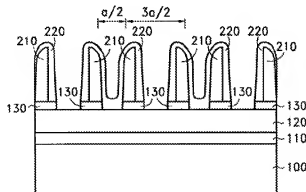


FIG. 6

Since Linliu et al. do not teach the step of transferring the resulting conformal layer structure to the substrate by etching, Linliu et al. do not teach each and every claim element of Claims 1, 10-14, 17, 22-24 and 30. As such, Linliu et al. fail to anticipate these claims under 35 U.S.C. §102(b). Accordingly, Applicants respectfully request the Examiner to withdraw this rejection.

Claims 1-4 and 6-33 are rejected under 35 U.S.C. 102(e) for allegedly being anticipated by Pontis et al. (U.S. Patent Application Pub. No. 2004/0136866). Applicants respectfully disagree with the Examiner but, solely in the interest of expediting prosecution, amend Claim1 in order to avoid this rejection.

Claim 1 is directed to a method of fabricating a nanostructure array comprising: providing a substrate having a top layer, depositing a sacrificial layer having a first etching characteristic directly on the top layer, patterning the sacrificial layer, forming a thin conformal layer having a second etching characteristic over the patterned sacrificial structure, wherein the first and second etching characteristics are different, anisotropically etching the conformal layer to create a pattern, removing the sacrificial layer, transferring the resulting conformal layer structure to the substrate by etching, and removing any remaining conformal layer structure, thereby creating at least one nanostructure in the top layer. Claims 2-4 and 6-33 depend from Claim 1.

Pontis et al. disclose a method of forming structures consisting of nanowire elements 626 and 628 on the surface of a silicon oxide insulation layer 604 which in turn is over a bulk silicon substrate layer 606 (see Figure 6, specifically Figure 6L). The method of Pontis et al. has the step of adding a masking layer 610 directly on top of the

nitride layer 608 (Fig. 6C). The structures eventually formed, nanowire elements 626 and 628, are composed of the material below the nitride layer 608 (Figs. 6K and 6L). As such Pontis et al. do not teach depositing a sacrificial layer having a first etching characteristic **directly on the top layer**.

Moreover, Applicants respectfully content that the Examiner's assertion "having a top layer (figure 6B, 608 or figure 6A, 602)" (page 4) is in error. Claim 1 recites a substrate having "a top layer", depositing a sacrificial layer directly on "the top layer", and creating at least one nanostructure in "the top layer". The Examiner asserts that in Pontis et al. both the 608 layer of material and the 608 layer of material are "a top layer". Applicants respectfully content that two separate and distinct layers cannot be the same "top layer".

Since Pontis et al. do not teach depositing a sacrificial layer having a first etching characteristic **directly on the top layer**, Pontis et al. do not teach each and every claim element of Claims 1-4 and 6-33. As such, Pontis et al. fail to anticipate these claims under 35 U.S.C. §102(e). Accordingly, Applicants respectfully request the Examiner to withdraw this rejection.

Rejections under 35 USC § 103

Claim 5 is rejected under 35 U.S.C. 103(a) for allegedly being obvious over Pontis et al. Applicants respectfully disagree with the Examiner but, solely in the interest of expediting prosecution, amend Claim1 in order to avoid this rejection.

Claim 5 depends from Claim 1 and is directed to a method of fabricating a nanostructure array of claim 3, wherein: the nanostructure comprises Si, and the reduction in dimension is accomplished by controlled XeF_2 etch.

For the reasons provided earlier, Pontis et al. do not teach or suggest depositing a sacrificial layer having a first etching characteristic **directly on the top layer**.

As Pontis et al. do not teach or suggest each and every claim element of Claim 5, Pontis et al. fail to render Claim 5 obvious under 35 U.S.C. §103(a). Accordingly, Applicants respectfully request the Examiner to withdraw this rejection.

CONCLUSION

In view of the foregoing remarks and amendment, Applicants respectfully submit that all of the claims are in condition for allowance, which action is requested. If in the opinion of the Examiner, a telephonic conference would expedite the prosecution of the subject application, Applicants encourage the Examiner to call the undersigned at (510) 486-4534.

If any further fee is required to maintain pendency of this application, the Commissioner is authorized to charge any necessary and additional fees, including fees for additional extensions of time that may be due to Deposit Account No. 120690, referencing Attorney Docket: IB-1997.

Respectfully submitted,

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By: /Robin C. Chiang/
Robin C. Chiang, Ph.D.
Reg. No. 46,619

Lawrence Berkeley National Laboratory
One Cyclotron Road, MS 56A120
Berkeley, CA 94720
Telephone: (510) 486-4534
Facsimile: (510) 486-7896